## Experimental demonstration of locally oxidized hybrid silicon-plasmonic waveguide

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## Experimental demonstration of locally oxidized hybrid silicon-plasmonic waveguide

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We experimentally demonstrate a self-aligned approach for the fabrication of nanoscale hybrid silicon-plasmonic waveguide fabricated by local oxidation of silicon (LOCOS). Implementation of the LOCOS technique provides compatibility with standard complementary metal-oxide-semiconductor technology and allows avoiding lateral misalignment between the silicon waveguide and the upper metallic layer. We directly measured the propagation and the coupling loss of the fabricated hybrid waveguide using a near-field scanning optical microscope. The demonstrated structure provides nanoscale confinement of light together with a reasonable propagation length of  $\sim\!100~\mu\mathrm{m}$ . As such, it is expected to become an important building block in future on-chip optoelectronic circuitry. © 2010 American Institute of Physics.

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For decades, silicon (Si) is known as the material choice for standard complementary metal-oxidesemiconductor (CMOS) electronics. Owing to its technological advantages and the high refractive index contrast between the Si core and the surrounding cladding material Si photonics is becoming an important platform for the realization of integrated, technologically compatible optical devices for guiding, modulation, and light manipulation on-chip. 1,2 However, limited by diffraction, the minimal size of photonic components cannot be scaled down in accordance with modern electronics. A promising approach to further miniaturize the dimensions of optical devices is to incorporate metallic features into the photonic circuitry. These metallic structures are designed to support well confined surface plasmon polaritons (SPPs) modes, thus paving the way for the implementation of subwavelength-scale on-chip optical systems.<sup>3-5</sup> In addition, due to the fact that microelectronic architecture is fundamentally metal-based, the Si-plasmonic devices can potentially carry both optical and electronic signals simultaneously on the same metal line, thereby presenting an opportunity for combining the data/bandwidth capacity and ultrafast optical signal processing of photonics with the miniaturization capability of plasmonics and electronics.

To attain the goal of plasmonic integrated circuits, various devices<sup>5–12</sup> and waveguiding schemes<sup>13–16</sup> were proposed and demonstrated. Unfortunately, the inherent drawback of plasmonic guiding is inevitable losses due to the mode interaction with the metal. A trade-off between localization of the optical mode and propagation loss exists in all plasmonic devices, namely, smaller mode size and higher confinement are usually accompanied by stronger interaction of the electromagnetic field with the metal resulting in a reduction in SPP propagation distance. Recently, the concept of hybrid plasmonic waveguide was outlined.<sup>17</sup> This hybrid structure consists of a high refractive index medium (e.g., silicon) that is separated from a metal surface by a thin gap of low refractive index spacer (e.g., oxide). In this configu-

ration, the electromagnetic energy resides in both the high and the low index materials and the guiding mechanism relies on both characteristics of plasmonic and photonic modes. As a result, by controlling the dimensions of the gap and the parameters of the high refractive index layer, the hybrid waveguide mode can be varied from plasmonic to photonic-like regimes, allowing a wide range of modal characteristics such as strong confinement and long propagation length to be accessible. The capability to compromise between nanoscale confinement and low loss characteristic makes the hybrid waveguide an attractive tool for future design of dense optoelectronic circuitry on-chip.

In this work, we present a self-aligned approach for the fabrication of hybrid plasmonic waveguides. Our hybrid plasmonic structure is fabricated by standard microelectronic process of local-oxidation of silicon (LOCOS), in which oxide spacers are created for electronic isolation between transistors in order to eliminate parasitic effects. Implementation of the LOCOS technique is compatible with standard CMOS technology and enables integration of optical components onto silicon-on-insulator (SOI) substrate with thin buried oxide layer (BOX=70 nm) currently used in modern electronics.<sup>21</sup> The LOCOS process can be tuned to precisely control the shape and the dimensions of the waveguide<sup>22</sup> and it allows avoiding lateral misalignment between the high index silicon waveguide and the metal surface. After the fabrication, we directly measured the propagation and coupling loss of the hybrid waveguide using near-field scanning optical microscope (NSOM).

The fabrication process is depicted in Fig. 1. We used a SOI (SOITEC) substrate consisting of 360 nm thick crystal-line silicon layer on top of a 2  $\mu$ m thick BOX. First, a 100 nm thick silicon nitride layer (SiN) was deposited by low-pressure chemical vapor deposition at 800 °C. Next, the mask defining the optical structure consisting of the a hybrid plasmonic waveguide, the input/output photonic waveguides, and a 1  $\mu$ m length tapered couplers for adiabatic conversion between the photonic and the hybrid mode <sup>23</sup> was patterned in protective SiN layer using standard electron-beam lithography followed by inductively coupled reactive ion etching

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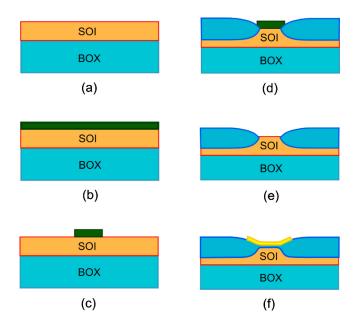


FIG. 1. (Color online) Fabrication process flow of the locally oxidized hybrid plasmonic waveguide. (a) Planar substrate; (b) nitride layer deposition; (c) nitride patterning; (d) local oxidation; (e) nitride strip; and (f) formation of thin oxide gap and metal deposition.

(RIE) with a CHF<sub>3</sub>/O<sub>2</sub> gas mixture. To transfer the defined pattern into the silicon, the chip was oxidized (wet process) at 920 °C where the nitride layer served as a mask preventing the oxygen diffusion. After oxidation the SiN was etched using an additional RIE step. The measured widths of the photonic and the hybrid waveguides is 500 nm and 310 nm, respectively. To obtain a low index spacer between the silicon waveguide and the metal we thermally grew a thin (75 nm) oxide layer. Finally, after second lithographic step design for opening a metallization window, a 50 nm thick gold layer was deposited onto the chip followed by a lift-off process to lay down the metallic strip of the hybrid plasmonic structure. It should be noted that the metal surface is selfaligned with respect to the thin oxide layer and the silicon waveguide underneath because the hybrid region is isolated and separated from the rest of the structure by thick oxide spacers defined with the LOCOS process.

To verify the profile of the hybrid waveguide we captured a scanning-electron microscope (SEM) micrograph of the hybrid plasmonic waveguide prior the metal deposition, as shown in Fig. 2(a). The obtained structure consists of a silicon rib waveguide (310 nm width, 325 nm height) with a thin oxide gap of 75 nm. The rib height is 150 nm. Using

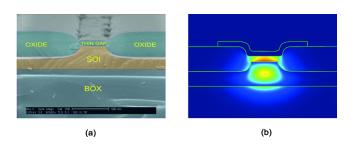


FIG. 2. (Color online) (a) SEM image of the hybrid plasmonic structure with highlighted different material layers. (b) Electromagnetic simulation showing the intensity profile of the mode in the hybrid plasmonic waveguide. We used the actual device dimensions as obtained from the SEM image.

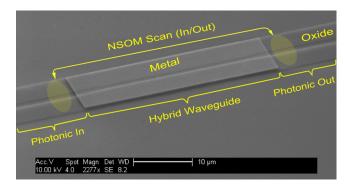


FIG. 3. (Color online) SEM micrograph (top view) of the hybrid plasmonic structure coupled to the photonic waveguides. The near-field scan areas are schematically marked by the shaded yellow ellipses on the image.

finite element mode solver we calculated the optical mode profile of the device [Fig. 2(b)] taking into account the following Cr/Au deposition of 5 nm/50 nm, respectively, and the actual dimensions of the optical structure as taken from the SEM image. According to the simulation, the effective index of the hybrid mode and its propagation loss parameter are 2.58 cm<sup>-1</sup> and 102 cm<sup>-1</sup>, respectively.

To experimentally characterize the loss of the device we fabricated hybrid plasmonic waveguides with different lengths while keeping the same dimensions of the tapered coupler region for adiabatic conversion between the photonic mode (where no metallic layer is placed on top of the structure) and the hybrid mode, namely, tapering of the waveguide width from 500 to 310 nm over a 1  $\mu$ m length. A transverse magnetic (out of plane) polarized light generated by a diode laser at 1.552  $\mu$ m wavelength was launched into the waveguides using a polarization maintaining lensed fiber with a mode size of 2.5  $\mu$ m. The light from the output facet of the waveguide was collected with a similar fiber and detected by an InGaAs photodetector (HP 81634A). To evaluate the propagation and coupling loss of the device we used NSOM (Nanonics MultiView 4000) that allows to directly measure the light intensity adjacent to the hybrid plasmonic structure (Fig. 3), thus eliminating the impact of the chip facets, different light coupling conditions and photonic waveguide imperfections on the measurement results. The NSOM measurements were also useful in measuring the mode profile of the light in the photonic waveguide, before and after the hybrid section.

Using a metal coated NSOM glass tip with an aperture diameter of 250 nm we measured the optical intensity at the input and the output of the hybrid plasmonic waveguides for different device lengths. Representative NSOM measurement results are shown in Fig. 4.

By calculating the ratio between the average light intensity at the input and the output of the device we obtained the attenuation of the optical signal as it propagates via the hybrid plasmonic structure. The results are presented in Fig. 5.

By performing a linear fit to the obtained data, the propagation loss of the hybrid waveguide was found to be  $105\pm5$  cm<sup>-1</sup>, very similar to the theoretical estimation of 102 cm<sup>-1</sup> calculated by the finite element approach. Using the intersection of the fit line with the *y*-axis we estimated the coupling efficiency between the photonic and the hybrid waveguides. We found the coupling loss to be  $1.7\pm0.2$  dB per interface.

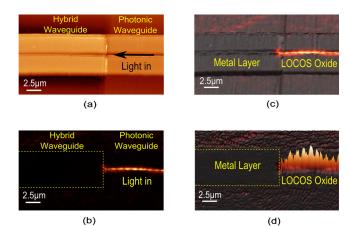


FIG. 4. (Color online) Representative NSOM measurement results of the device. (a) Topography image; (b) NSOM image; (c) three-dimensional (3D) representation of the superimposed topography and NSOM images; and (d) 3D representation of NSOM image.

In summary, we experimentally demonstrated the fabrication and the measurements of hybrid plasmonic waveguides realized by local oxidation process. Implementation of the LOCOS technique for device fabrication prevents lateral misalignment at the hybrid (metal–oxide–silicon) interface and provides smooth waveguide sidewalls. Taking advantage of local intensity measurement using a near-field optical microscope we directly characterized the propagation and the coupling loss of the device. Owing to its

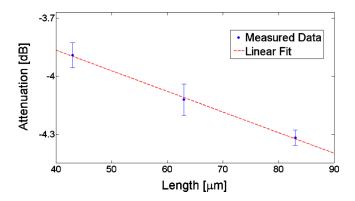


FIG. 5. (Color online) Light intensity attenuation as a function of length as derived from the near-field characterization. The error bars represent the standard deviation of three independent experiments. The dotted line shows the linear fit to the measurements.

promising characteristics of nanoscale light confinement together with a relatively long propagation length, the hybrid silicon-plasmonic waveguide can potentially become an important building block in future on-chip optoelectronic circuitry.

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