Local Isolation of High-Voltage Photovoltaic Cells Using Buried Layers of Oxidized Porous Silicon

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***Abstract*—In this paper, we have developed a simple method to isolate epitaxially grown thin silicon film using micrometer thick layers of buried porous silicon. The process is based on formation of trenches within epitaxial p-type Si layer that was grown on top of a p^+-type Si (100) wafer. Either electrochemical or galvanic etching in hydro-fluoric solutions procedures were employed to etch the p^+-type silicon under and around the trenches, at the interface of the substrate and the epi-layer, and to transform the etched material into buried PSi. Electrical characteristics of the formed isolation, called "local isolation by buried oxidized PSi", have been measured. The isolation resistance of the subsequently oxidized PSi film was found to increase by 3–6 orders of magnitude up to the level of few GΩ (GigaOhms). Finally, this procedure has been exploited to demonstrate a miniature *photovoltaic solar array* where two photovoltaic cells were connected in series using the laser-induced forward transfer metallization process, as a model for high voltage photovoltaic solar cell.**

***Index Terms*—High-voltage photovoltaic cells, local isolation, porous silicon, solar cells.**

I. Introduction

THE use of porous silicon (PSi) [1], [2] for electrical isolation between microelectronic devices on a given Si chip has been extensively studied in the past [3]–[8]. Oxidized PSi, having better isolation has been considered to be an alternative to the "local oxidation of Si" (LOCOS) technology [9] and more general isolation needs [10]–[13]. Nevertheless, LOCOS has become the dominant isolation technology because of excellent interfaces between the thermal-oxide and Si, superb electrical isolation, and the ease of fabrication. Another considered approach was "full isolation by porous silicon" (FIPOS) [14], [15]. FIPOS technology (trench etch and oxidized PSi formation) was successful in silicon-on-isolator (SOI) applications; but other SOI technologies were advantageous since they allowed better interfaces of silicon with the buried oxide. The use of FIPOS remained limited to applications that required deep oxide regions (e.g., in power transistors which use oxidized macro PSi based thermal isolation in microelectromechanical systems [MEMS] circuits [15]).

The recent progress in MEMS, integrated optics, and silicon-based solar cells technology increased again the interest in porous silicon and FIPOS. This is also supported by the availability of advanced substrates with high quality epitaxial layers and progress in deep trench etching techniques and corresponding tools. Recently, the utilization of the PSi technology to photovoltaic (PV) applications has been considered by several groups [16]–[24]. In particular, PSi can be utilized to create "black silicon" (a term related to a Si surface having nearly zero-reflection over a broad spectral region of the solar spectrum and over a wide range of incident angles [17]–[19]) and as a layer to facilitate detachment of the formed solar cells from the carrier substrates in order to use these substrates repeatedly [19]–[21].

Here, we report on a novel FIPOS type isolation, mainly for PV applications, that we name: "local isolation by buried oxidized PSi" (LISOP). It is different from the previous solutions by 1) using specially engineered epitaxial silicon structures, 2) advanced etch and oxidation processes, and 3) special device layouts that enable formation of highly efficient solar cells. The proposed method enables us to substitute costly SOI wafers by much cheaper, ordinary PV-grade Si wafers to fabricate variety of devices such as high-voltage PV (HV-PV) solar cells where only local isolation is required.

In brief, the starting material for the LISOP method is a prepatterned Si substrate having trenches over those regions of the substrate where local isolation is going to be formed. The use of p-type Si layers over p^+ substrates greatly simplifies the process (a similar LISOP process can also be developed for n-type Si substrates). The prepatterned substrate is placed in hydro-fluoric (HF) acid solution to activate a selective etching and formation of PSi at the bottom of the trenches. Two approaches have been developed and will be described hereafter. The first is based on

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an electrochemical (EC) etching at the bottom of the trenches to create a buried, local layer of PSi. In this case, the process is activated by external current source connected in between the top electrode (inside the HF solution) and the metal electrode at the backside of the Si wafer [1], [2]. The second approach is based on galvanic etching (GE) where the entire wafer is immersed into the HF solution with oxidant molecules such as H_2O_2. When the metallic back contact is reduced it closes the necessary electrical connection between the top prepatterned Si surface and the backside metal electrode (without the use of an external current source; see Section II-A) [25]–[27]. Both methods and the experimental results are described in the next section.

II. Formation of a Buried Local Isolation by Buried Oxidized Porous Silicon Isolation

A. Electrochemical Etching of Porous Silicon Layers

EC etching of a Si wafer requires a controllable potentiostat that can deliver moderate currents, standard EC cell (made of Teflon) for HF:Ethanol (ETOH) solution and a Pt electrode immersed in the EC solution. The main advantage of the EC etching process is its relatively high speed (from few nm/min up to few μm/min), high level of film's thickness control and good lateral uniformity [2]. In addition, by controlling the current, one can easily vary the porosity and the size of the pores [1], [2]. While currently a single wafer EC processing technology has been utilized, recent developments suggest that batched EC processing is also possible [22]. This topic, however, is outside the scope of the current work.

The Si wafers used here are heavily doped p^+ Si substrates (0.01–0.02 Ω·cm) with a top epi-layer of lightly doped p-type Si (1–10 Ω·cm; 4 μm in thickness). Standard deep dry etching process (Bosch process) has been exploited to define 4 μm deep and 2 μm wide trenches. A 0.7 μm silicon nitride (SiN) hard mask has been used during the Bosch process to define the trenches in the top epi-layer only. Additional 100 nm thick chemical vapor deposition (CVD) SiN layer was deposited on the surface of the trenches. This layer was etched off by reactive-ion-etching to clear/remove the bottom of the trenches. SiN spacers remained at the walls of trenches. Thus, electrical contact was enabled between the EC solution and the heavily doped substrate, exposed at the bottom of the trenches.

Next, samples were placed in a standard EC cell that was operated in the "galvanostatic" mode, i.e., under constant current conditions. The process typically proceeds for 50–500 s. As a result, PSi has been *selectively* created at the bottom of the trenches where the EC solution is in contact with the heavily doped Si substrate. Fig. 1 presents few cross-sectional SEM images to show that porous structures having a "mushroom-like" profile are created at the bottom of the trenches. These figures also demonstrate that almost no etching of the epi-layer takes place. The current density is about 50 mA/cm^2 in (a) and (b), and only 2 mA/cm^2 in (c) and (d).

The mushroom-like PSi films at the bottom of the trenches (see Fig. 1(a) and (c)) indicate that most of the EC current flows toward the heavily doped (having low-resistivity) substrate with practically no etching of the lightly doped epi-layer. The smaller the EC current density, the lesser is the porosity of the PSi film. In Fig. 1(a) and (c), the distance between the trenches is 12 μm so that the etching time is not sufficient to generate a connected network of "mushrooms," while in [Fig. 1(b) and (d)] the distance between the trenches is 5 μm and the mushrooms merge, to create a complete, continuous porous film about 3–4 μm deep, under the epi-layer within the substrate. Note that the epi-layer thickness (4 μm) was dictated by the expected visible light absorption depth (for PV applications) and the technical limitations dictated by the need for high quality trenches formation.

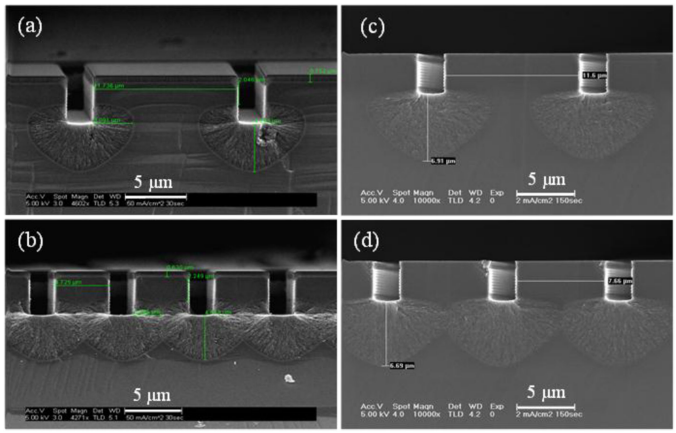

Fig. 1. Cross-sectional SEM images of the buried PSi mushrooms, created at the bottom of 4 μm deep trenches. (a, b) EC etching at a current density of 50 mA/cm^2 for 30 s; in (a) the distance between the trenches is 12 μm and the PSi mushrooms do not merge, while in (b) the distance between the trenches is 5 μm and the mushrooms merge. (c, d) Similar images for the case of a current density of 2 mA/cm^2 etched for 150 s. Here again, merging is obtained for a distance of 5 μm (between trenches) but not for 12 μm. Notice that in both cases the top epi-layer has practically not been etched.

B. Galvanic Etching of the Buried Porous Silicon Layers

The GE to produce PSi layers is based on the chemical oxidation–reduction reaction at the interface of the metallic back contact and use of the HF- H_2O_2 oxidant solution. The reaction proceeds via generation of holes at the metal-covered (silver alloy) side as the result of the metal interaction with H_2O_2. The holes that were generated diffuse to the opposite side of the silicon wafer, to stimulate silicon etching process in the HF-based solution. A demonstration of the employment of the GE process (using a Si wafer having the same pattern of trenches as that described in Section II-A) is shown in Fig. 2. As in the EC process described above and in Fig. 1, here as well the etching process does not take place within the epi-layer. This is demonstrated in the expanded image in Fig. 2(e). Fig. 2(a) demonstrates the result of a short time (2 min) GE, where the mushroom is located under the trench only, while at longer etching time (Fig. 2(b)) of 8 min all neighbor mushrooms were merged.

The GE process produces 10–20 nm diameter pores. Unlike the EC process, it is difficult to vary the size of the created pores. The etching rate is somewhat slower than in the EC method, however, the main advantage of the GE process is the possibility

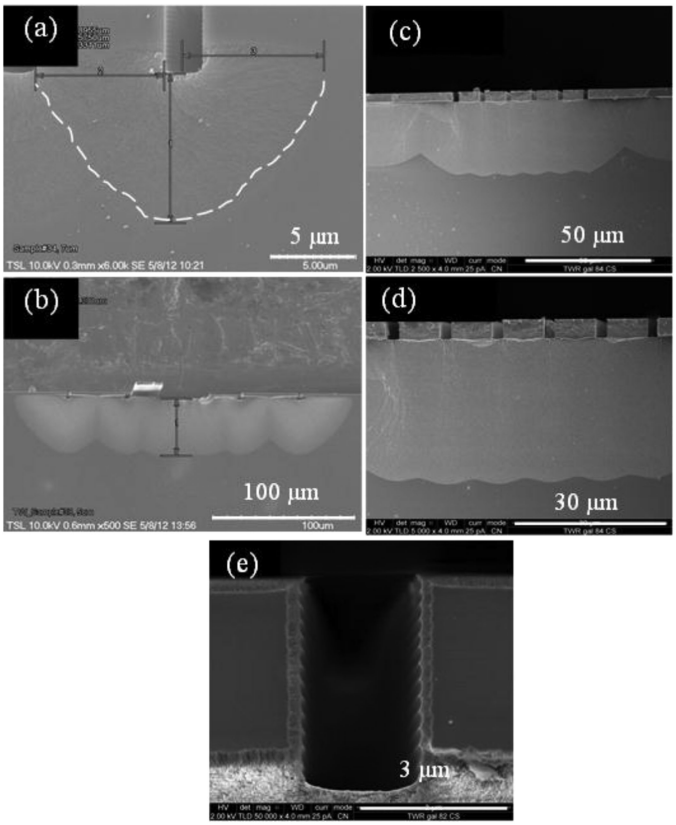

Fig. 2. GE process. The difference in GE time is demonstrated for trenches separated by 8 micrometers: (a) 10 min etching, PSi depth of 9 μm, (b) 60 min etching, PSi depth of 42 μm. (c, d) GE etching for 10 min using samples that were partially protected by an oxide layer in addition to the nitride. The etching depth is 30 μm. (e) Enlarged image of a trench to demonstrate the lack of any etching within the top (epi) layer because of the nitride layer protection surrounding it.

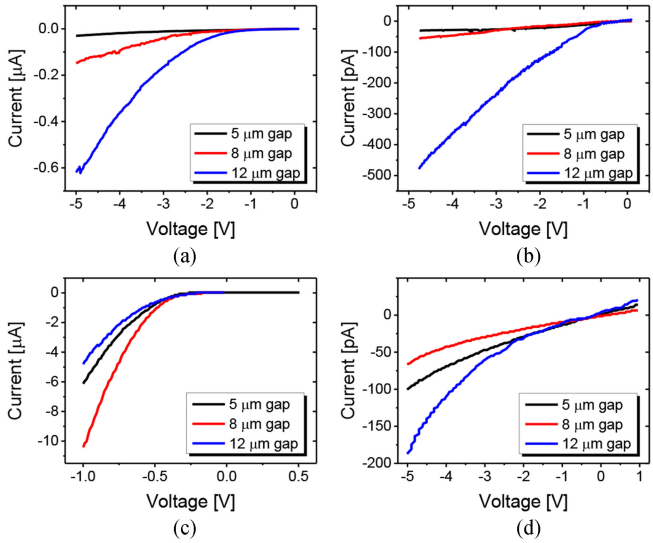

Fig. 3. Current–voltage characteristics of buried PSi isolation for different widths of isolated epi-silicon structures: (a, c) before and (b, d) after oxidation. (a, b) PSi fabricated by the GE method; (c, d) PSi fabricated by the EC method. Notice the different current scales of (a, c) μA for nonoxidized samples and (b, d) pA for oxidized PSi.

to perform a batch, parallel processing: One may insert many wafers into the wet hood, resulting in a significant increase of the throughput. SEM cross sections of PSi structures fabricated by GE are shown in Fig. 2(c) and (d) for GE time of 10 min. The etching depth is equal to 30 micrometers. Maximum isolation has been achieved for trenches separated by 5 μm, which have been used hereafter.

C. Oxidation and Isolation Resistance Measurements

The purpose of the buried PSi film is to provide local electrical isolation between the top epi-Si layer (where PV junctions are going to be defined) and the heavily doped Si substrate. To fabricate high voltage solar cells, created by connecting PV diodes in series on single epi-silicon islands (= fingers; such a finger is created by two trenches on its sides and the oxidized PSi beneath), it is necessary to isolate both sides of the formed p–n junctions. To achieve maximum isolation, we have performed a 10 min EC oxidation of the buried PSi using 1 M sulfuric acid EC solution at the current density of 20 mA/cm^2. Both EC and GE etched PSi films were oxidized at essentially the same conditions.

Current–voltage (I-V) measurements were performed to determine the isolation resistance of the PSi layer. A probe station with a picoAmpere (pA) current resolution has been used. As a reference, we have used a bare silicon substrate with the epi-layer on top of a p^+ bulk Si wafer. Following the measurements of the reference sample (with the epi-Si fingers having a length of 100 μm), the probe electrodes were moved to isolated fingers, e.g., island fingers defined by two side trenches and bottom isolated PSi films created by the EC/GE etching and oxidation processes. We were able to perform resistance measurements on different sections of the same p^+ substrate having 5, 8, and 12 μm wide stripes (= separation distance between the trenches). The results, shown in Fig. 3(a) and (b) for the GE process, demonstrate that upon the completion of the 10 min GE, the isolation resistance of the sample increased from 10^4–10^5 Ω (without etching) to 10^7–10^8 Ω following the etching process.

The oxidation step further increases the isolation resistance up to 10^{10}–10^{11} Ω (see Fig. 3(b) and (d) for the GE and EC processes, respectively). This level of isolation resistance is sufficiently large to replace standard SOI wafers in applications such as high voltage PV and, most probably, in a much wider scope of semiconductor applications such as MEMS [15]. The isolation resistance (around the zero-voltage origin) for these oxidized PSi films can be estimated to be (70 $\pm$ 30) GΩ for all separations where the thickness of the PSi films is about 30 μm.

Similar results were measured for the EC process (Fig. 3(c) and (d) with the isolation resistance raised from about 10^4–10^5 Ω prior to EC etching up to 10^6–10^8 Ω after EC etching at a current density of 2 mA/cm^2 for 300 s (thus a PSi layer of approximately 5–6 μm in thickness is created). After EC oxidation (at a current density of 20 mA/cm^2 for 10 min) the isolation resistance increases up to 10^{10}–10^{11} Ω, which is very close to the limits of our measurement system. Here again, we have estimated the resistance to be (100 $\pm$ 50) GΩ for all separations.

Notice that at higher voltages (close to -4 V) the *I-V* curves of Fig. 3(d) show a nonlinear behavior that is typical to a current breakdown. This allows estimation of the breakdown dielectric strength of the oxidized PSi to be about $\sim 10^4$ V/cm.

III. High Voltage Photovoltaic Cells With Local Isolation by Buried Oxidized Porous Silicon Isolation

A. High-Voltage Photovoltaics

High-voltage PV sources have a variety of applications including solar energetics, voltage supplies for portable consumer products, solar chargers, MEMS drivers, etc. [28]. There are two conventional approaches to create high-voltage solar voltage supplies [28]–[32]. The first approach is to use low-voltage (single p–n junction) PV elements and DC–DC boost converters capable to increase the low-level input voltages to the needed voltage level. This approach requires a complicated analog circuit, and faces many challenges related to cost and system complexity. The second conventional approach is to connect the individual solar cells (p–n junctions) in series. Under standard 1.5AM sunlight illumination, most Si PV p–n diode cells generate a voltage of about 0.5 ± 0.1 V. Connecting in series allows voltages to reach at the level of hundreds of Volts (limited by the breakdown voltages of the insulating layers). The connection of PV elements can be external, if the solar cells are on separate platforms. This is what can be found in most commercial solar energetics systems. It is clear that external connection strongly increases the system cost and decreases reliability. In addition, when light concentrators are used, the problem of parallel connections becomes critical since the total current from the solar system can reach tens of Amperes or more. HV solar cells solve this problem by decreasing the current for the same amount of light power per unit square of the solar array surface.

HV solar arrays that comprise lateral photodiodes were demonstrated in the layer of polysilicon on shallow trench isolation oxide in a standard CMOS process flow [29]. This solution allows high voltages to be obtained, but the PV quantum efficiency is low because of the strong electron–hole recombination in polysilicon. HV solar cells on crystalline silicon substrate using SOI isolation were reported in [15], [28], and [32]. The photosensitive diodes were connected in series by metal plugs. The efficiency of light conversion is relatively high, but this solution is expensive because of the high cost of the SOI starting material.

We have exploited the idea described in the previous sections (e.g., the process of LISOP isolation) to create HV array of solar cells by connecting in series fully isolated individual PV diodes at the wafer-level, using a standard silicon wafer instead of a SOI substrate. LISOP isolation was formed from the sides and under the individual PV cells (silicon arrays of p–i–n junctions with i- related to intrinsic silicon) with trenches in both sides. The process flow includes: 1) deep-trench etch (4 μm in depth) through the 4 μm thick epitaxial Si (epi-layer), reaching the p^+ Si substrate (0.1–0.01 $\Omega\cdot$cm), 2) EC/GE etching processes to convert the p^+ substrate into PSi at the bottom of the trenches, and 3) oxidation of the PSi films using EC oxidation with H_2SO_4 acid solution. The structure of the final device is schematically shown in Fig. 4.

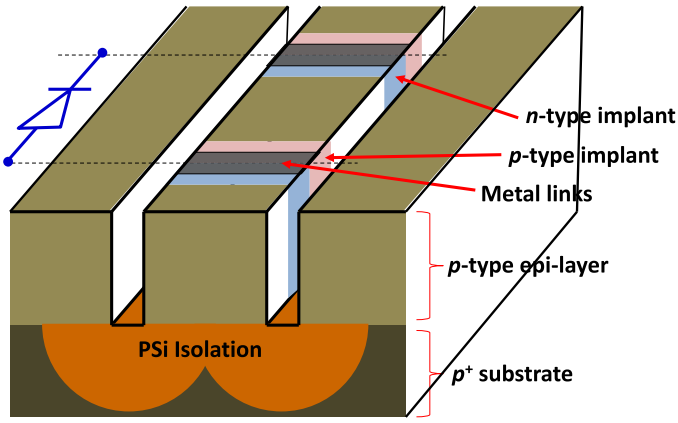

Fig. 4. Design of HV solar cells array (here only two diodes (cells) are depicted as a model) using LISOP isolation: A schematic view of the outcome of the LISOP isolation process.

At first, a p-type Si epi-layer (4 μm thick in our feasibility study) was grown on top a p^+ Si substrate. Next, Si arrays (fingers in the epi-layer) were implanted, n-type first (using Phosphorous ions; dose: 8×10^{15} cm^{-2}, energy of 20 keV, baked at 1150 °C for 3 h) and then, Boron-ion implanted (dose: 8×10^{15} cm^{-2}, energy: 7 keV, baked for 1 h) to obtain the p-type side of the diodes. Next, trenches were etched between the PV cell arrays and around the whole structure. The trenches cut through the Si epi-layer down to the p^+ Si substrate. The surface of the entire structure is oxidized to suppress surface recombination. p–i–n junctions formed after implantations (blue and pink areas in Fig. 4) are connected one to the other using silicide-butted contacts (gray) or by a conductive paste. In the first case, the trenches are filled with dielectric followed by chemical mechanical polishing to expose the Si surface. If required, the entire structure might be lifted and removed from the Si wafer by etching the oxidized PSi (e.g., using HF solution), similar to a process described in reference [17].

A benefit of the proposed solar cell (besides cost) is that the associated fabrication steps can be easily integrated into the standard process flows (e.g. established Complementary metal–oxide–semiconductor (CMOS) and Micro- electro- mechanical systems (MEMS) processes) requiring only very few additional masks. This enables relatively low-cost, low power PV arrays that can be integrally formed as part of the integrated circuit. It is clear that within a CMOS integration scheme, connection between the single cells can be done also by Vias.

B. High-Voltage Solar Cell With Local Isolation by Buried Oxidized Porous Silicon: Feasibility Demonstration

In order to demonstrate the feasibility of the LISOP isolation process and a formation of an HV-PV solar cell, like the one schematically shown in Fig. 4, we have performed the following. At first, a set of isolated p–i–n PV diodes were fabricated using the LISOP process described in the previous sections (e.g., definition of trench's pattern, EC etching and oxidation to create

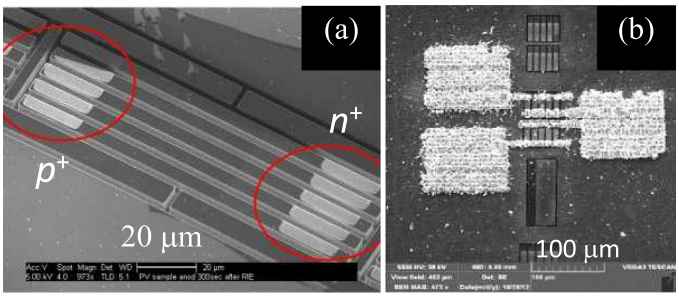

Fig. 5. (a) Five columns of p–i–n PV diodes separated (and isolated from each other) by trenches. The red circles mark the n+ and the p^+ regions of ion implantation. (b) Final device after LIFT metallization, connecting two rows in series.

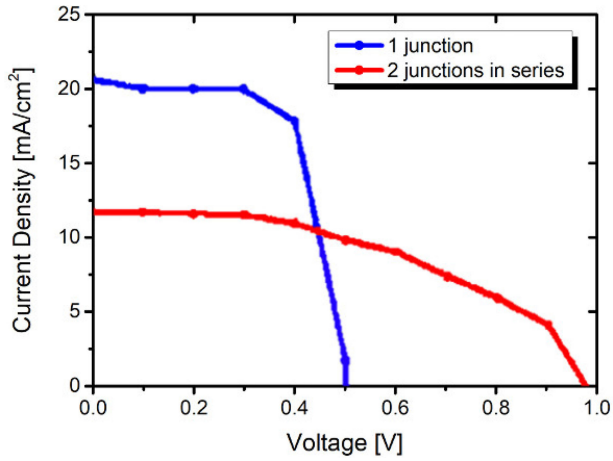

Fig. 6. Results showing current–voltage characteristics under illumination (1 Sun, AM1.5) and PV parameters (see below, Table I) measured for a single junction and for two junctions connected in series via LIFT.

connected film of oxidized PSi at the bottom of the trenches). Top-view SEM image of the final pattern, where red circles mark the ion-implanted regions (both n^+ and p^+), is shown on Fig. 5(a). Next, in order to realize the HV-PV cells, one needs to fabricate metal bridges over deep trenches to connect the PV diodes in series. We have chosen to utilize the laser-induced forward transfer (LIFT) technique [33]–[36], which is a direct-write printing technique that allows a deposition of tiny amount of metals onto a receiving substrate. More details about this technique, particularly its utilization for solar cells metallization, can be found in [33].

Fig. 5(b) shows the final device after printing narrow metallic lines of aluminum using LIFT. The width of the slightly granular but well conducting narrow stripes is about (10 ± 5) μm, which is the best resolution that can be obtained by this technique. The narrow stripes connect five columns of diodes in parallel and two rows in series. In addition, three external connection pads ($\sim 100 \times 100$ μm^2) were printed.

Finally, we have characterized the PV device in the dark and under illumination (1 Sun, AM1.5). Measurements were performed for a single-cell and two-cells in series configurations. The results, shown in Fig. 6, evidently show the expected PV effect under illumination. From these plots, the PV parameters including the open-circuit voltage $(V_{\rm OC})$, the short-circuit current density $(J_{\rm SC})$, the fill factor (FF), and the PV efficiency, were deduced and are summarized in Table I. Clearly, the open-circuit voltage increases from about $\sim$0.5 V for a single cell up to about $\sim$0.98 V for two-cells connected in series. Notice that the efficiency obtained for a single row of diodes is about 6.7% and 6.2% for two rows connected in series. These results are comparable with high voltage cells created using standard SOI technology and metallization techniques reported in [28], [29].

TABLE I
SUMMARY OF PV PARAMETERS FOR A SINGLE AND DOUBLE JUNCTIONS

	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
Single diode	0.50±0.03	20.7±0.1	62.4	6.7±0.4
Two diodes	0.98±0.03	11.8±0.1	46.0	6.2±0.4

IV. CONCLUSION

Simple methods to form buried electrically isolating layers based on PSi etching techniques, (both EC and GE), had been developed. The experiments performed in order to determine the geometry of PSi in terms of its depth and lateral dimensions had been discussed. Isolation resistance measurements confirmed that the buried oxidized PSi layers are characterized by fairly high isolation resistance, beyond 10^9 Ω. Preliminary results and the optimization of the oxidation process of the buried PSi layers suggest that further increase of isolation resistance is feasible, reaching conditions of practically open-circuit. We have been able to demonstrate that parallel connection of PV cells into HV arrays using simple metallization schemes and the development of oxidized PSi (LISOP) isolation is feasible. The proposed LISOP-PV technology can be considered to be a cheap and simple alternative to the standard, SOI wafers based, HV-PV cells technology that had been reported to generate higher voltages utilizing standard semiconductor industry (FAB) techniques [29].

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